

Revision : 1.3

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24	COM/LPT/F_USB
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[illegible]

A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.

A vertical line is shown. A horizontal arrow points from the line to a point labeled **B**. Another horizontal arrow points from the line to a point labeled **C**, which is located above point **B**.

A

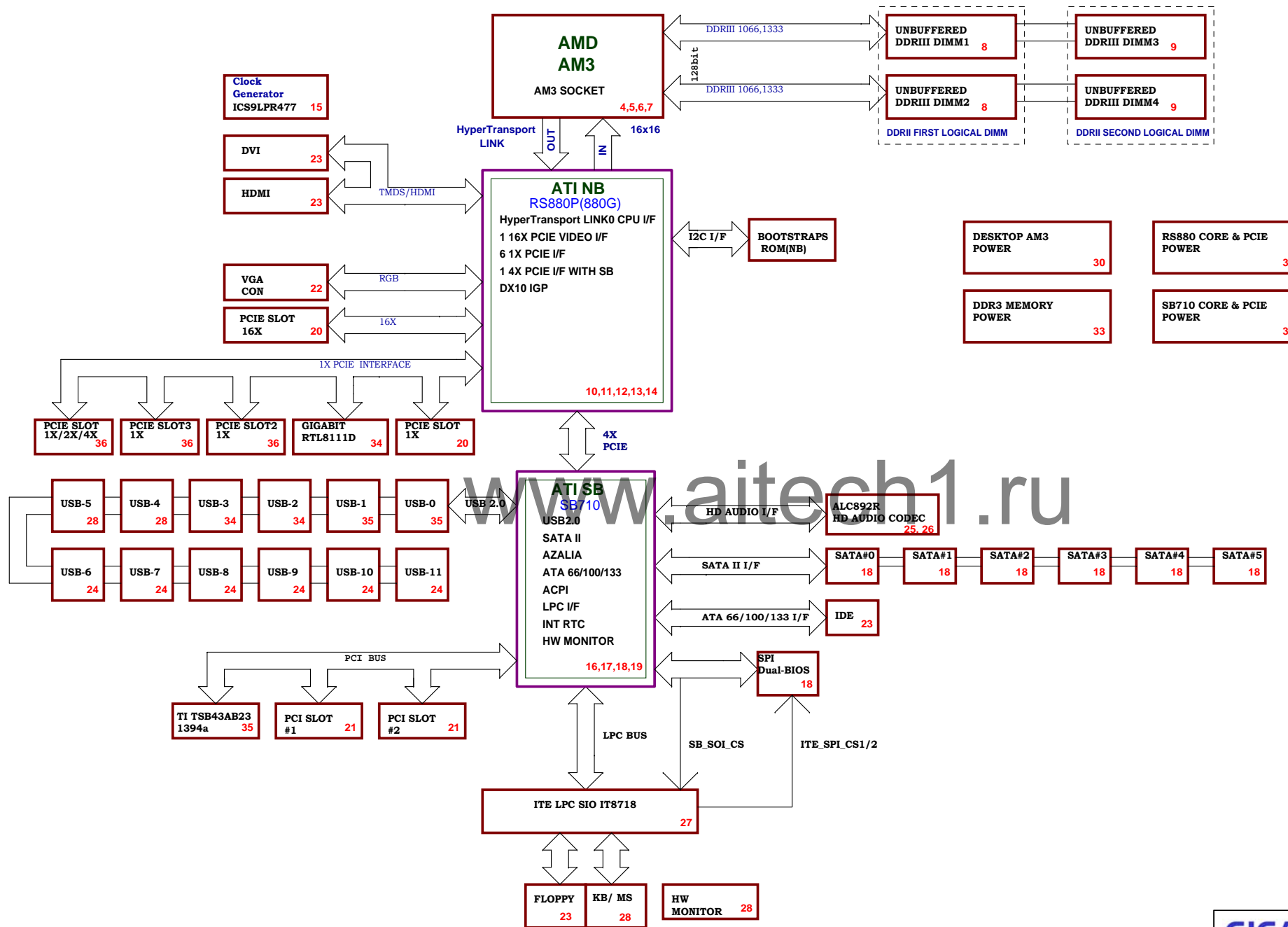
1

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3

A vertical number line with points A, B, C, and D. Point A is at the bottom, followed by B, then C, and D at the top. The segments AB and CD are marked with single tick marks, while segment BC is marked with a double tick mark. An arrow points to point C.

RS880 CUSTOMER DESKTOP REFERENCE DESIGN



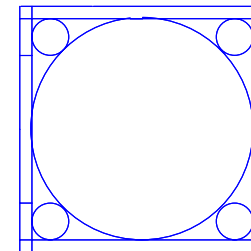
L0_CADIN_L[0..15] <L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 10

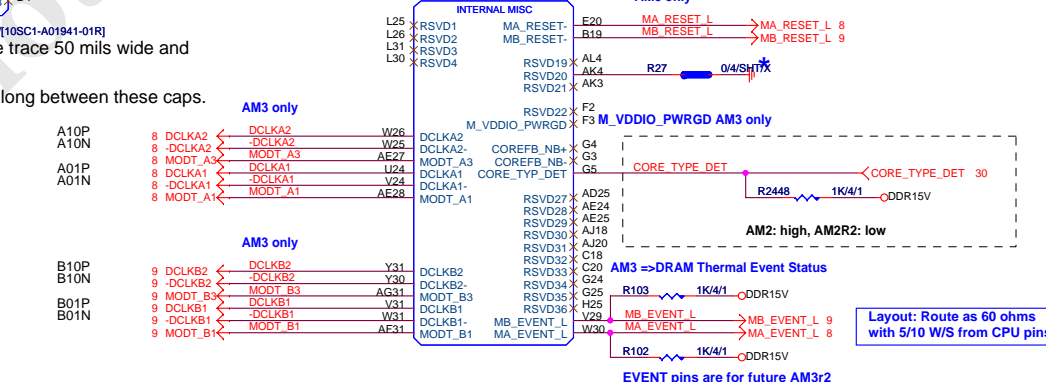
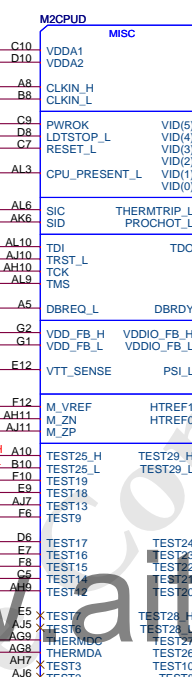
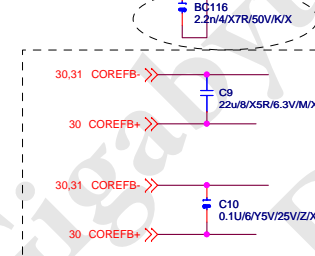
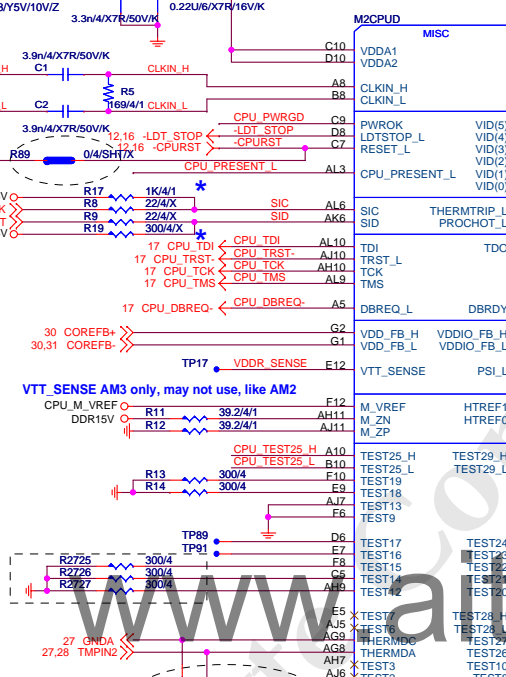
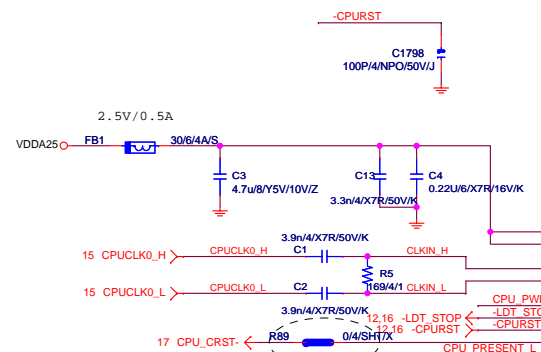


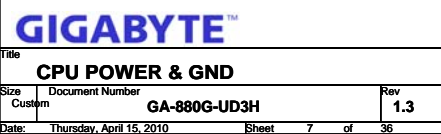
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

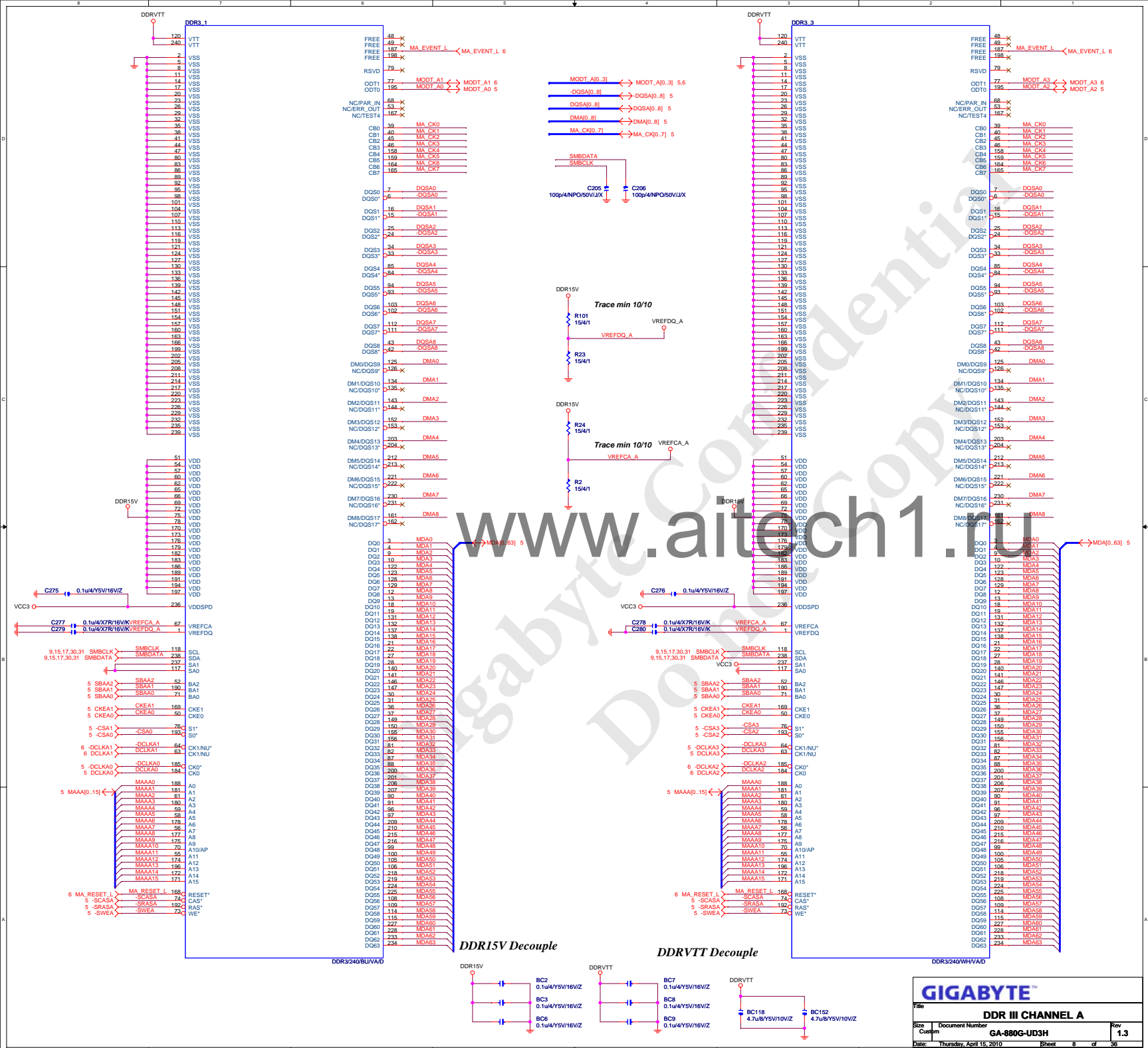
VLDT_A = VCC12_HT
VLDT_B = HT12B

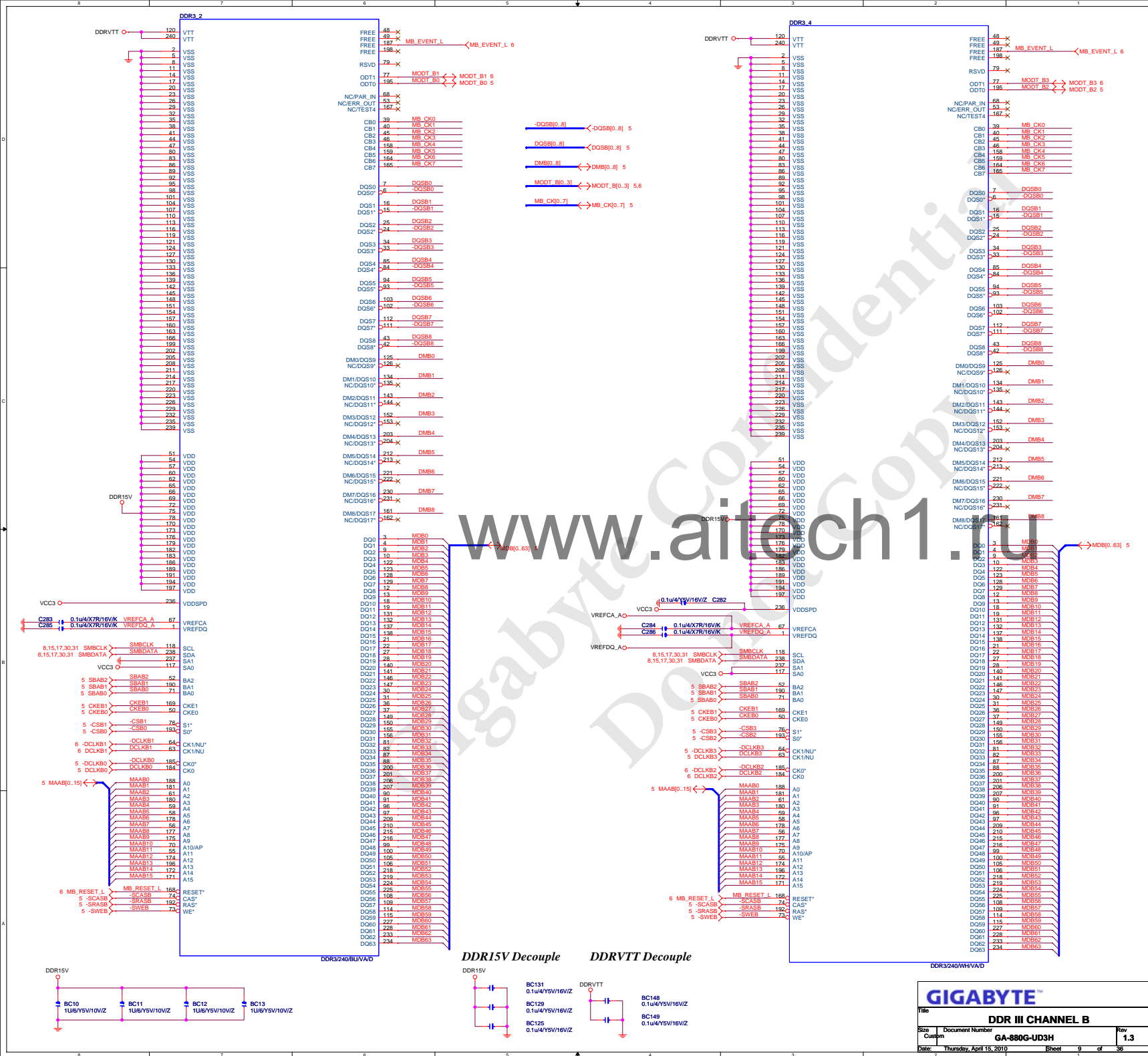
M2CPU
AM2RM/PP/BU/PB[12KRC-04K812-11R_12KRC-04K812-12R]

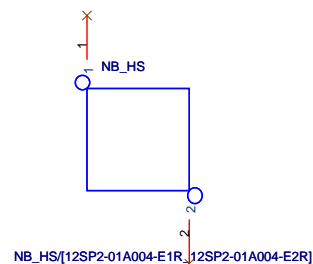
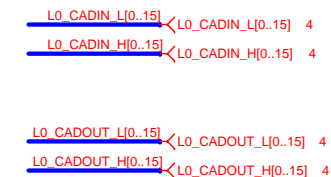






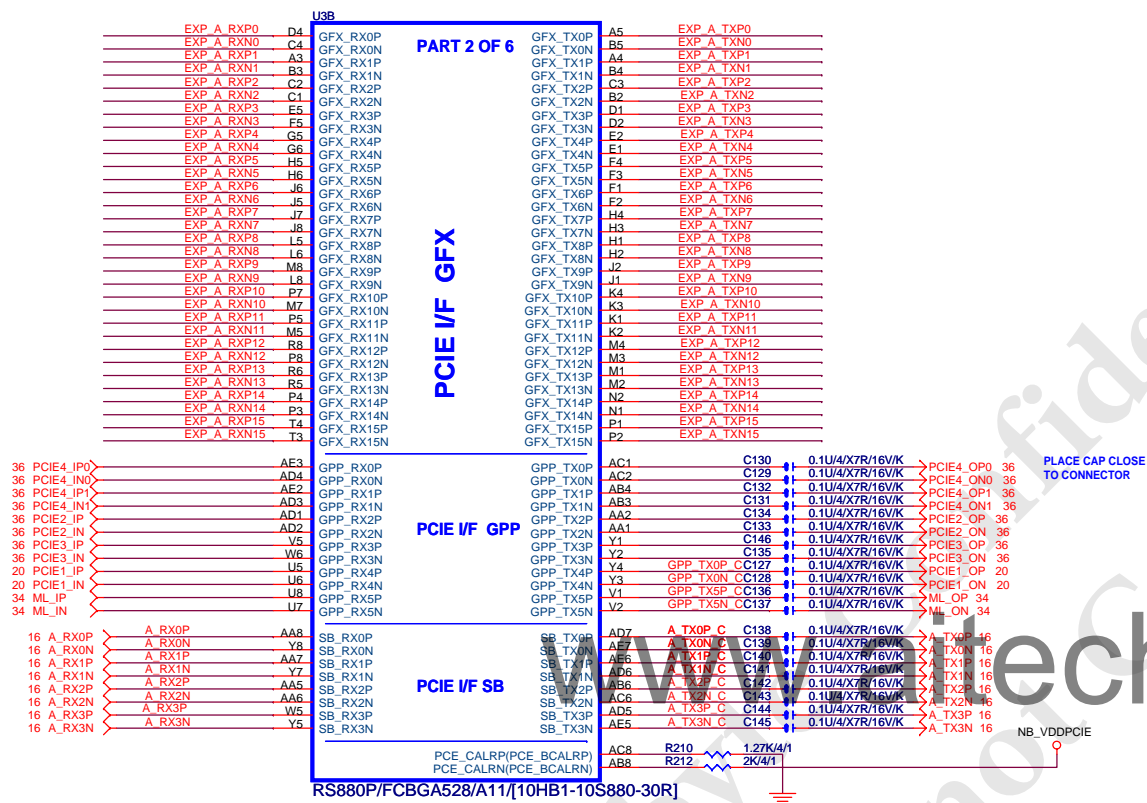


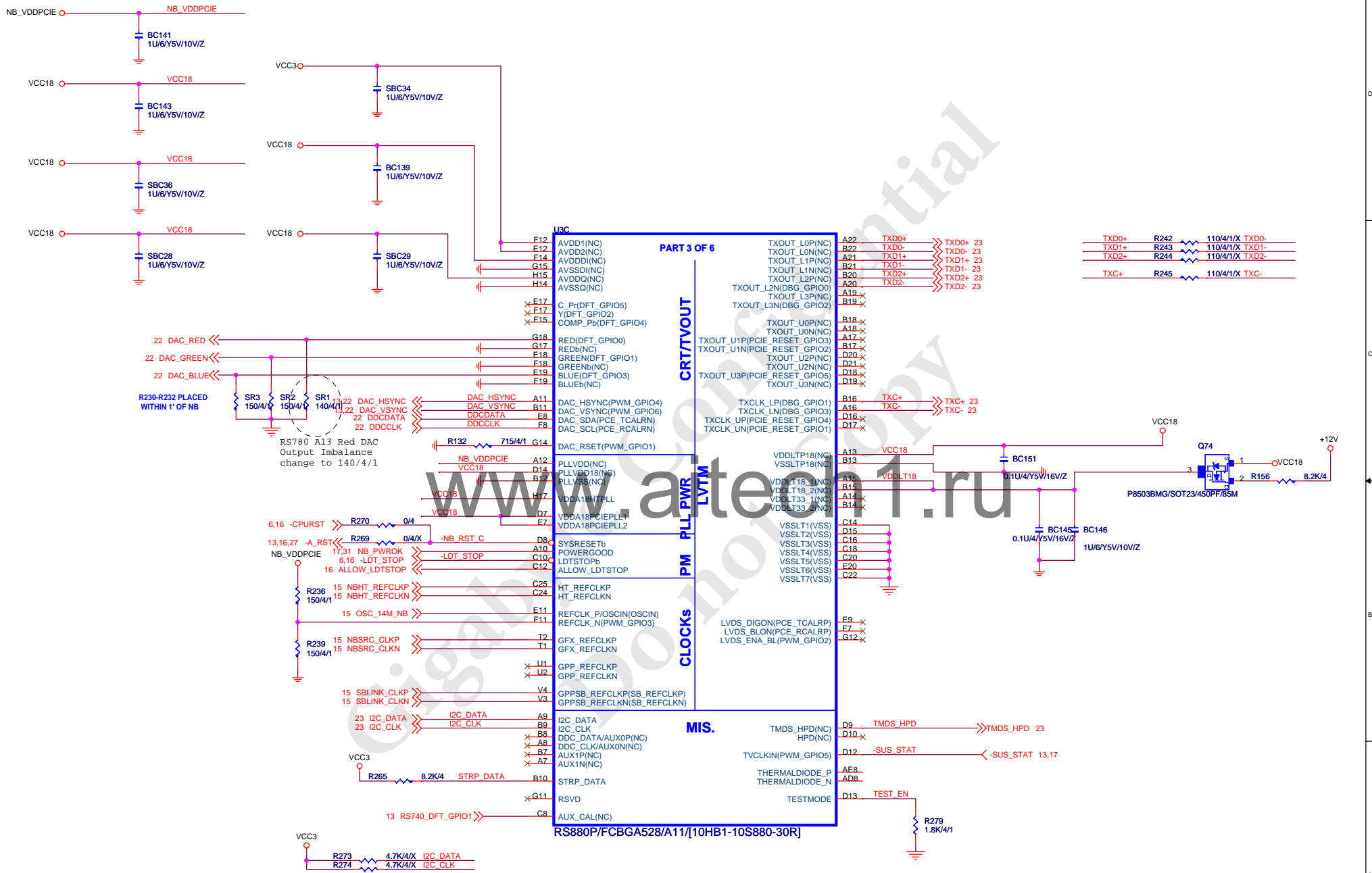


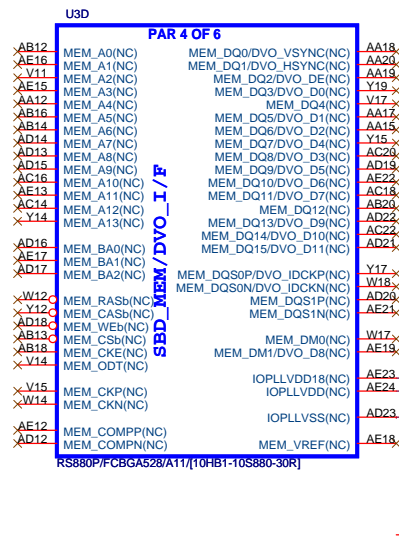


GIGABYTE™			
Title RS880 HT-LINK I/F			
Size B	Document Number GA-880G-UD3H		Rev 1.3
Date:	Thursday, April 15, 2010	Sheet 10 of	36

EXP_A_RXP[0..15] >> EXP_A_RXP[0..15] 20 EXP_A_TXP[0..15] >> EXP_A_TXP[0..15] 20
EXP_A_RXN[0..15] >> EXP_A_RXN[0..15] 20 EXP_A_TXN[0..15] >> EXP_A_TXN[0..15] 20

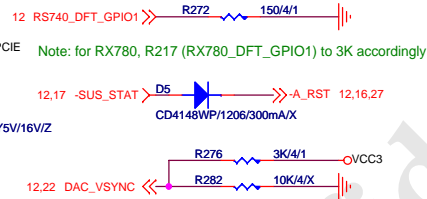






RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8



Note: for RX780, change following pull-down resistor to 3K accordingly

R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)



Note: for RX780, change following pull-down resistor to 3K accordingly

R219 (RX780_DFT_GPIO0)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EPROM if connected, or use default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable (RS740/RS780); Disable (RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

These pin straps are used to configure PCI-E GPP mode.

111: register defined (register default to Config E) default
110: 4-0-0-0-0 Config A
101: 4-4-0-0-0 Config B
100: 4-2-2-0-0 Config C
011: 4-2-1-1-0 Config D
010: 4-1-1-1-1 Config E
others: register defined (default to Config E)

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B

RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

1-1-1-1-1-1 Mode L default
1-1-1-1-1-1 Mode L
2-0-2-0-2-0 Mode C2
2-0-2-0-1-1 Mode K
2-0-1-1-1-1 Mode E
1-1-1-1-1-1 Mode L
4-0-0-0-1-1 Mode C
4-0-0-0-2-0 Mode B

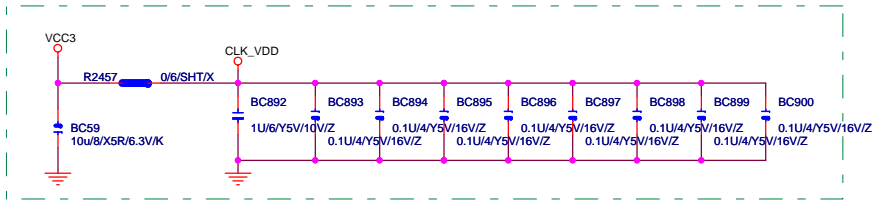
RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC
RX780: Not Applicable

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

Enables Test debug bus using PCIE bus
1. Disable (can be enabled thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register setting only
RS740: Not supported

GIGABYTE™



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

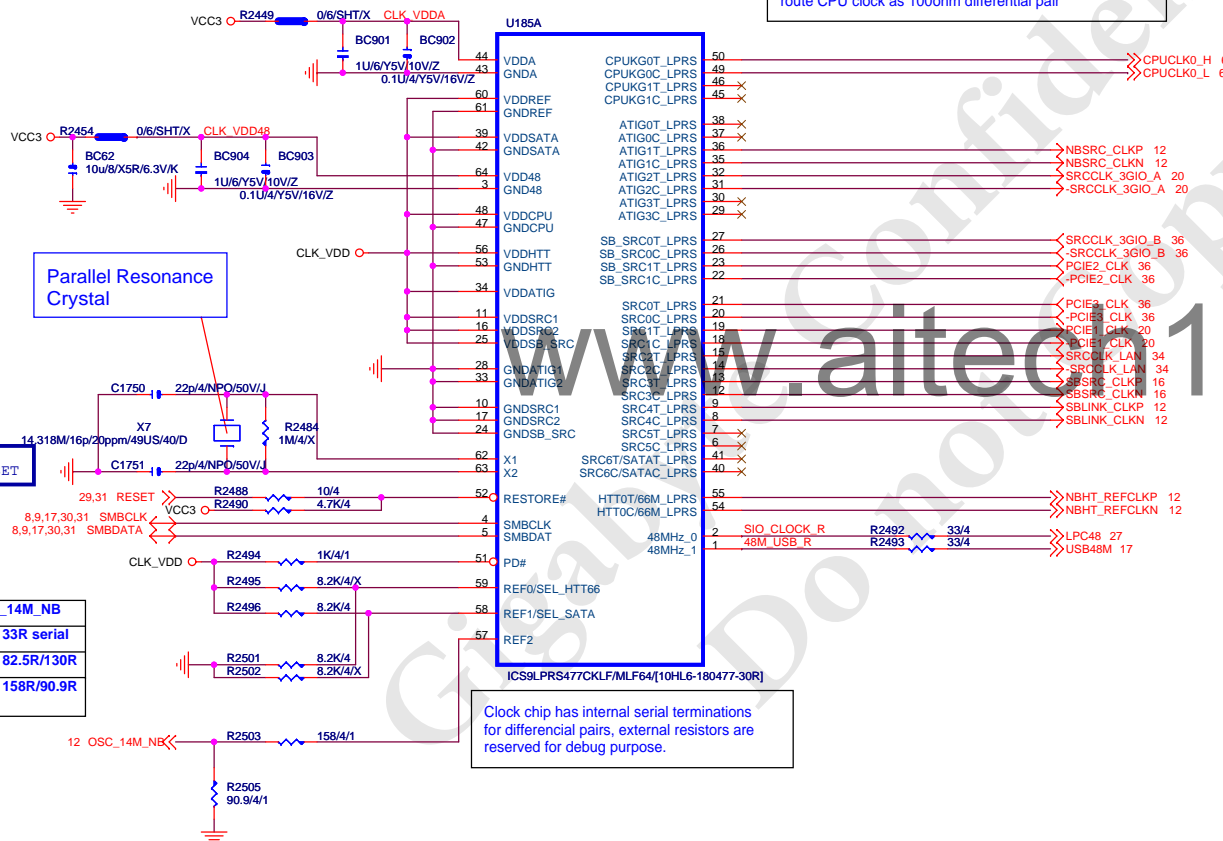


Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

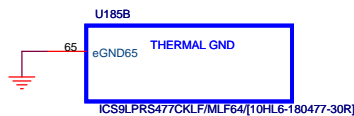


	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

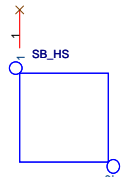
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



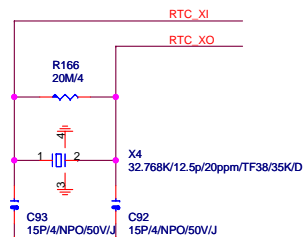
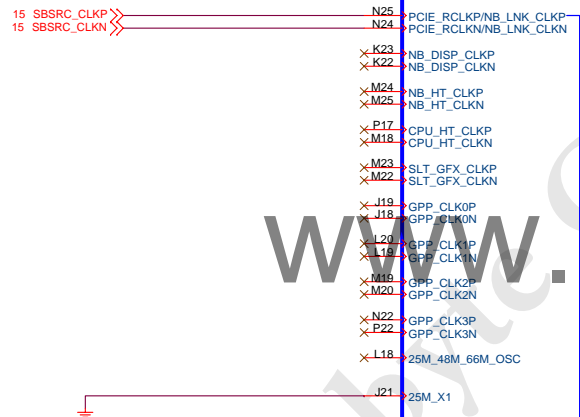
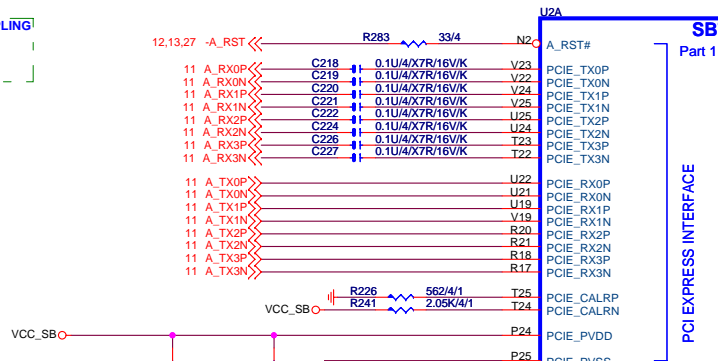


PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK



SB_HS[12SP2-030030-51R_12SP2-030030-52R_12SP2-030030-53R]



SHW/D0.64*5.08*6.74

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

SB700

Part 1 of 5

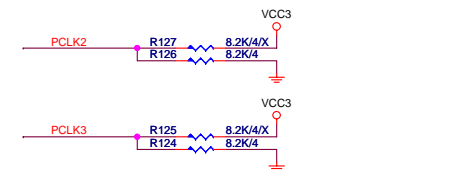
PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

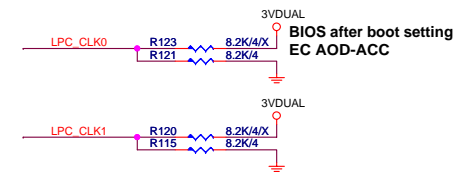
LPC

RTC



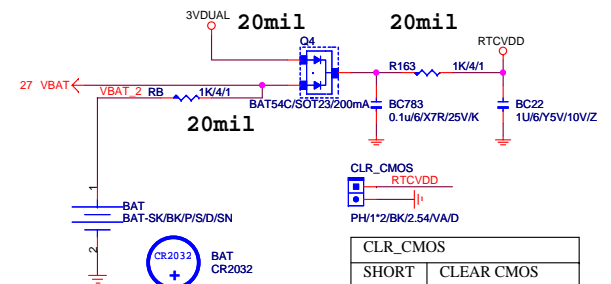
PULL HIGH
WATCHDOG TIMER ON NB_PWRGD ENABLED
USE DEBUG STRAPS

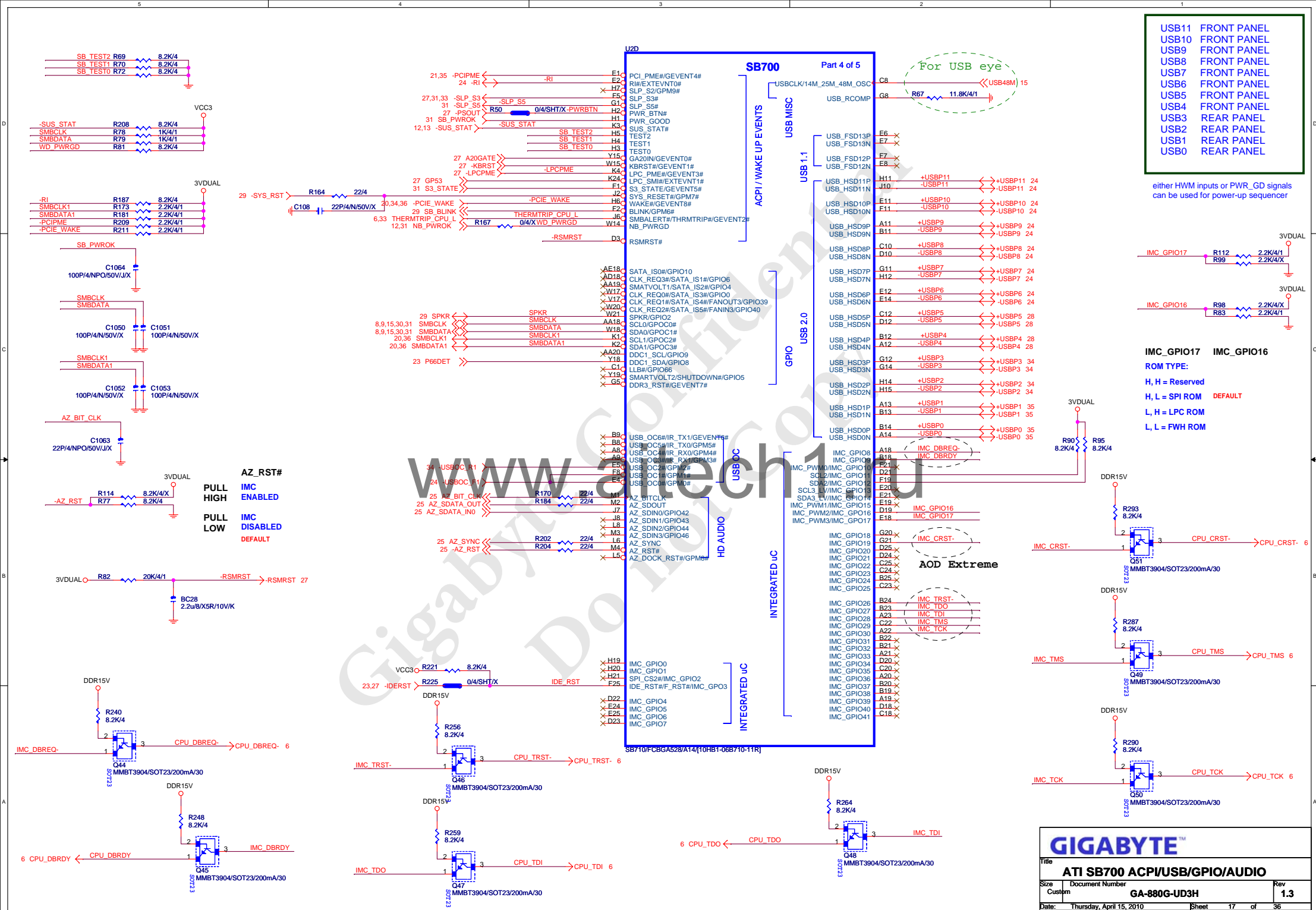
PULL LOW
WATCHDOG TIMER ON NB_PWRGD DISABLED
IGNORE DEBUG STRAPS

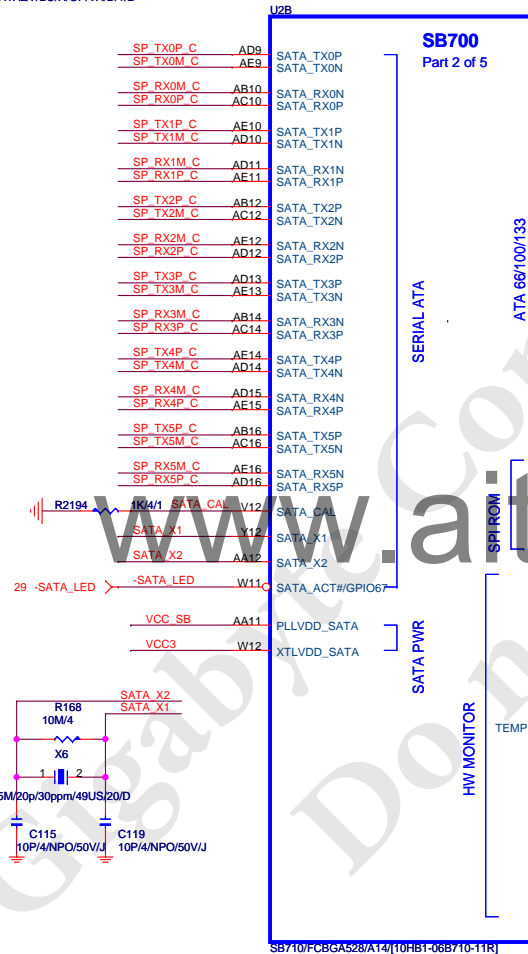
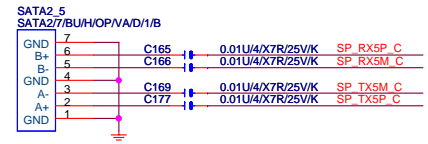
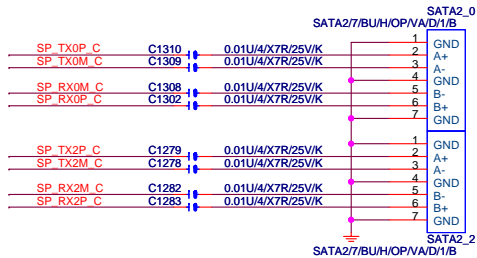


LPC_CLK0
Rev.A12
IMC ENABLED
CLKGEN ENABLED
AOD Extreme
IMC DISABLED
CLKGEN DISABLED
DEFAULT

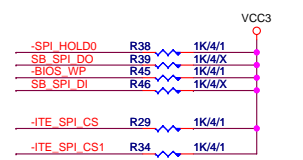
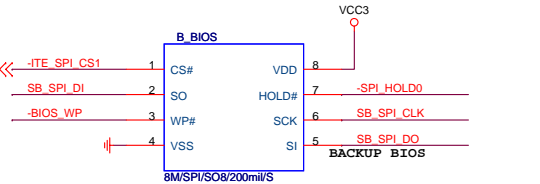
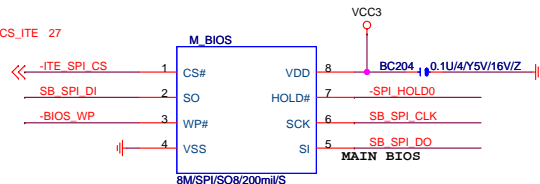
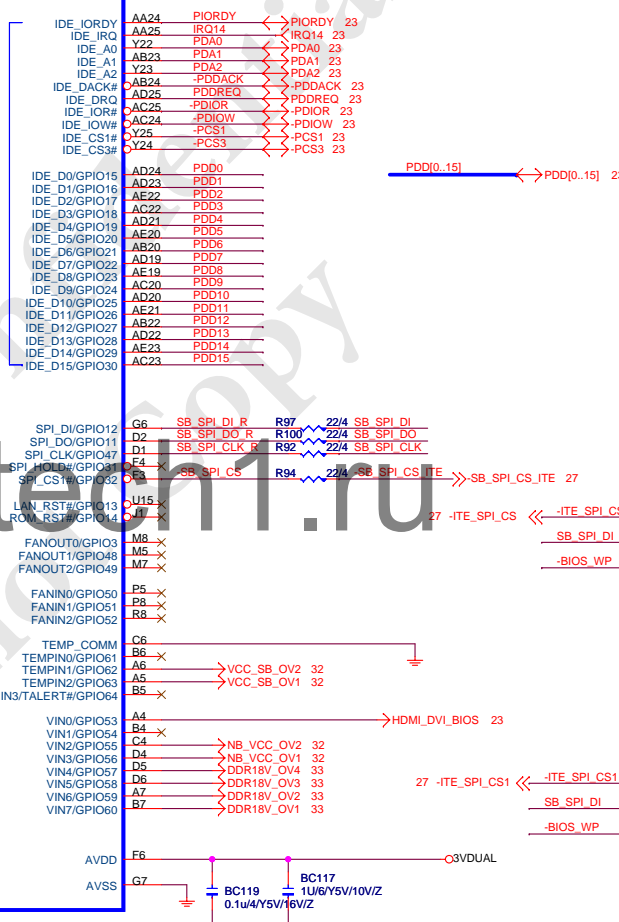
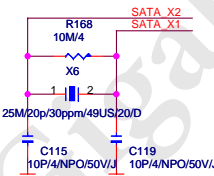
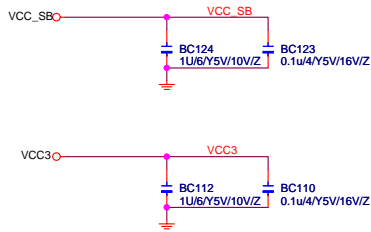
LPC_CLK1
CLKGEN ENABLED
CLKGEN DISABLED
DEFAULT





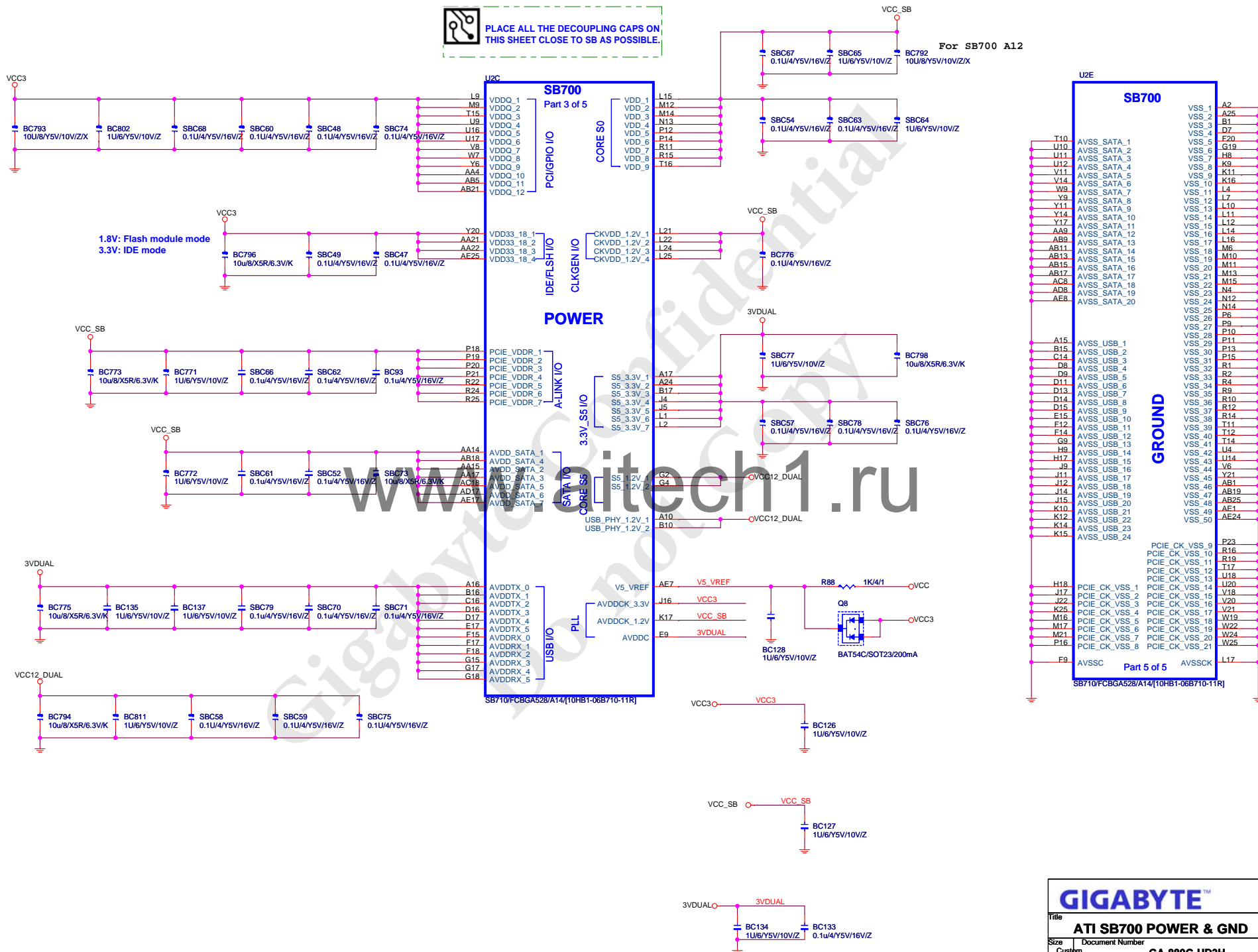


NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK





PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

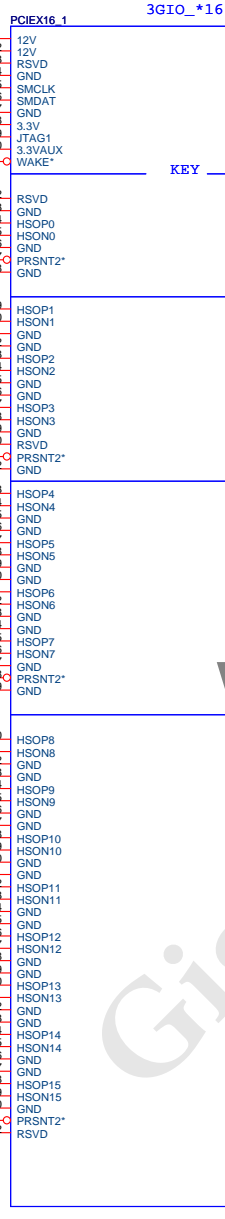


Lay 在 PCIe slot 旁
+12V ISEN R16 MASK-10
0/6/SHT-10/MASK/X
17,36 SMBCLK1
17,36 SMBDATA1

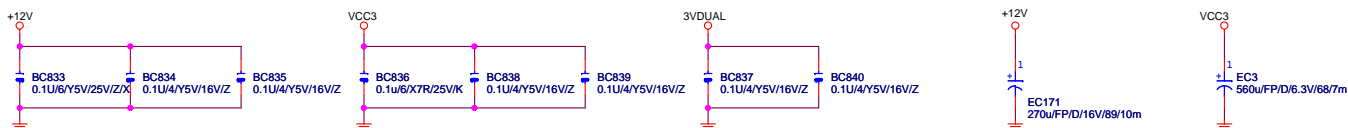
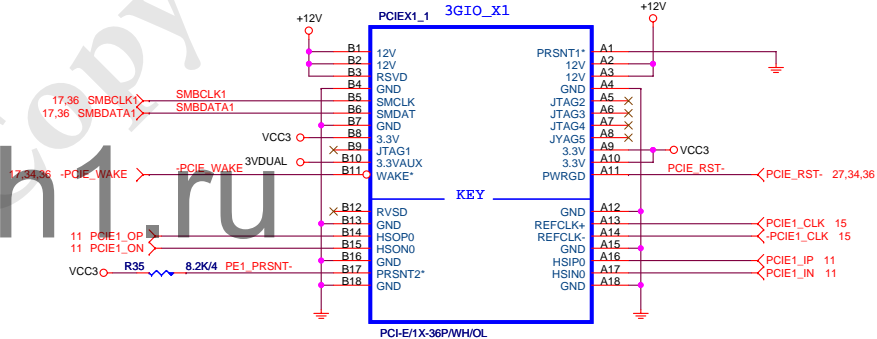
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EXP_A_RXN[0..15] >> EXP_A_RXN[0..15] 11
EXP_A_TXP[0..15] >> EXP_A_TXP[0..15] 11
EXP_A_TXN[0..15] >> EXP_A_TXN[0..15] 11

EXP_A_TXP0	C1644	0.1U4/X7R/16V/K	EXP_A_TXP0C
EXP_A_TXN0	C1645	0.1U4/X7R/16V/K	EXP_A_TXN0C
EXP_A_TXP1	C1646	0.1U4/X7R/16V/K	EXP_A_TXP1C
EXP_A_TXN1	C1647	0.1U4/X7R/16V/K	EXP_A_TXN1C
EXP_A_TXP2	C1648	0.1U4/X7R/16V/K	EXP_A_TXP2C
EXP_A_TXN2	C1649	0.1U4/X7R/16V/K	EXP_A_TXN2C
EXP_A_TXP3	C1650	0.1U4/X7R/16V/K	EXP_A_TXP3C
EXP_A_TXN3	C1651	0.1U4/X7R/16V/K	EXP_A_TXN3C
EXP_A_TXP4	C1652	0.1U4/X7R/16V/K	EXP_A_TXP4C
EXP_A_TXN4	C1653	0.1U4/X7R/16V/K	EXP_A_TXN4C
EXP_A_TXP5	C1654	0.1U4/X7R/16V/K	EXP_A_TXP5C
EXP_A_TXN5	C1655	0.1U4/X7R/16V/K	EXP_A_TXN5C
EXP_A_TXP6	C1656	0.1U4/X7R/16V/K	EXP_A_TXP6C
EXP_A_TXN6	C1657	0.1U4/X7R/16V/K	EXP_A_TXN6C
EXP_A_TXP7	C1658	0.1U4/X7R/16V/K	EXP_A_TXP7C
EXP_A_TXN7	C1659	0.1U4/X7R/16V/K	EXP_A_TXN7C
EXP_A_TXP8	C1660	0.1U4/X7R/16V/K	EXP_A_TXP8C
EXP_A_TXN8	C1661	0.1U4/X7R/16V/K	EXP_A_TXN8C
EXP_A_TXP9	C1662	0.1U4/X7R/16V/K	EXP_A_TXP9C
EXP_A_TXN9	C1663	0.1U4/X7R/16V/K	EXP_A_TXN9C
EXP_A_TXP10	C1664	0.1U4/X7R/16V/K	EXP_A_TXP10C
EXP_A_TXN10	C1665	0.1U4/X7R/16V/K	EXP_A_TXN10C
EXP_A_TXP11	C1666	0.1U4/X7R/16V/K	EXP_A_TXP11C
EXP_A_TXN11	C1667	0.1U4/X7R/16V/K	EXP_A_TXN11C
EXP_A_TXP12	C1668	0.1U4/X7R/16V/K	EXP_A_TXP12C
EXP_A_TXN12	C1669	0.1U4/X7R/16V/K	EXP_A_TXN12C
EXP_A_TXP13	C1670	0.1U4/X7R/16V/K	EXP_A_TXP13C
EXP_A_TXN13	C1671	0.1U4/X7R/16V/K	EXP_A_TXN13C
EXP_A_TXP14	C1672	0.1U4/X7R/16V/K	EXP_A_TXP14C
EXP_A_TXN14	C1673	0.1U4/X7R/16V/K	EXP_A_TXN14C
EXP_A_TXP15	C1674	0.1U4/X7R/16V/K	EXP_A_TXP15C
EXP_A_TXN15	C1675	0.1U4/X7R/16V/K	EXP_A_TXN15C

PCIE_RST-
C1643
100P4/N/50V/X



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File
PCI EXPRESS X 16, X1

Size
Custom

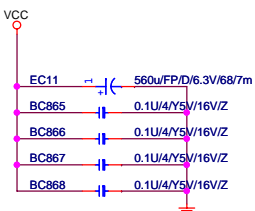
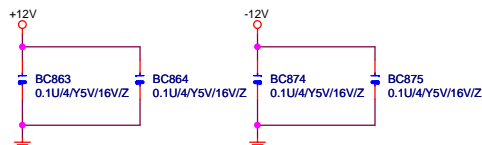
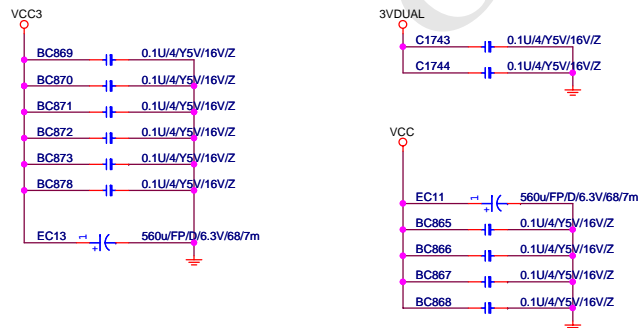
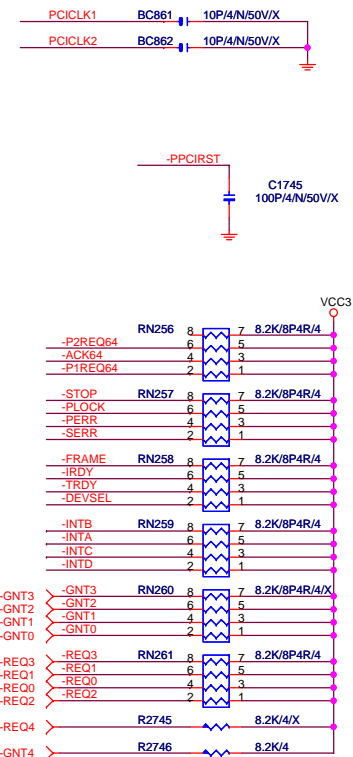
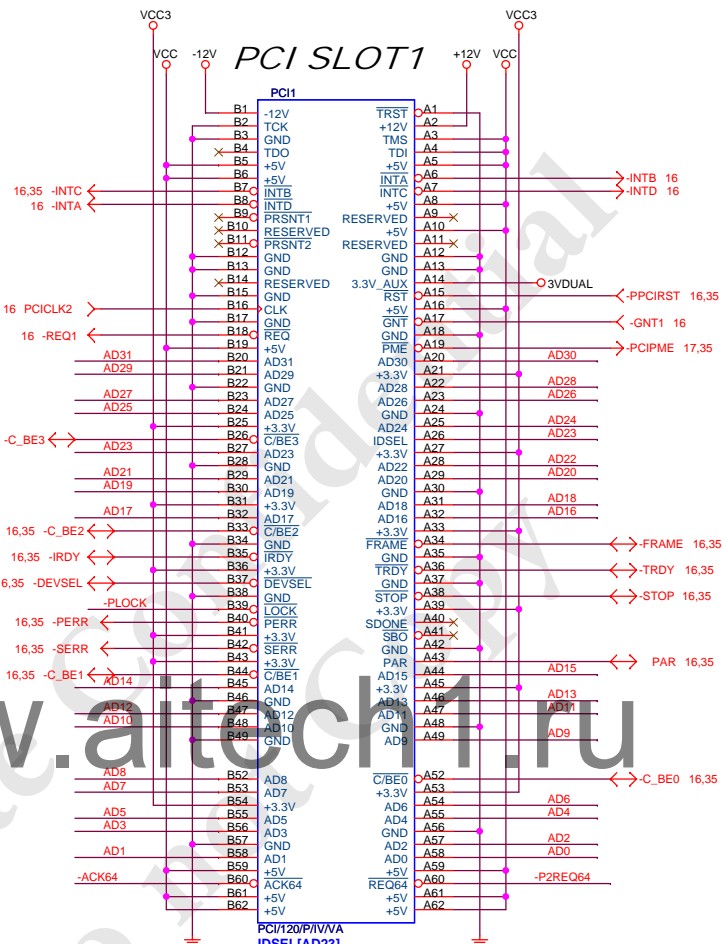
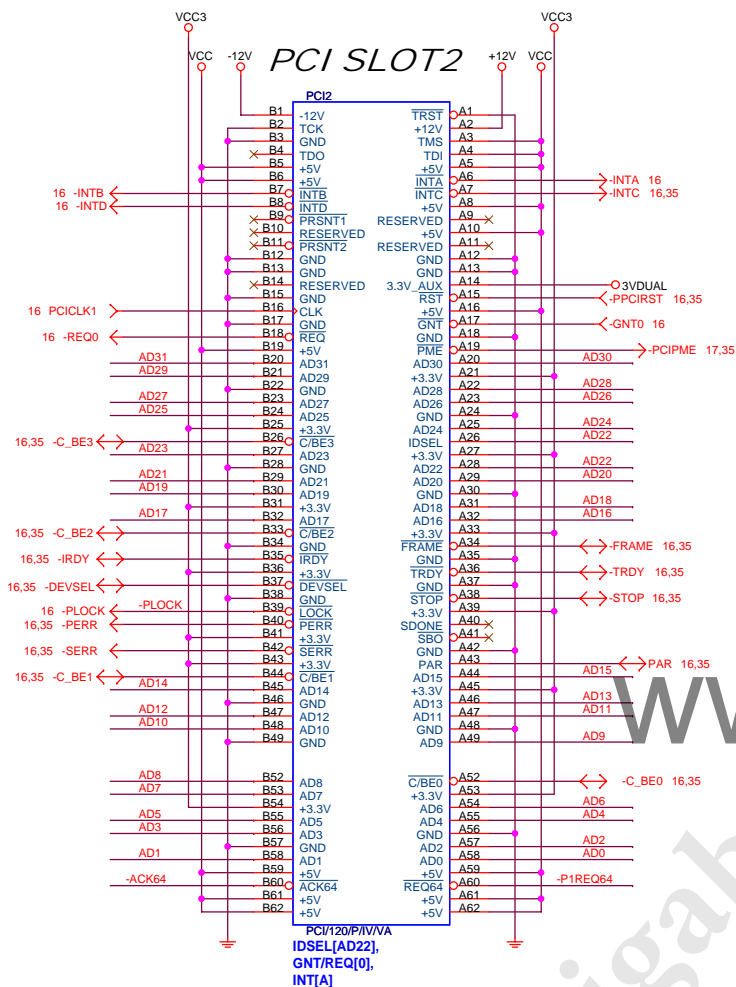
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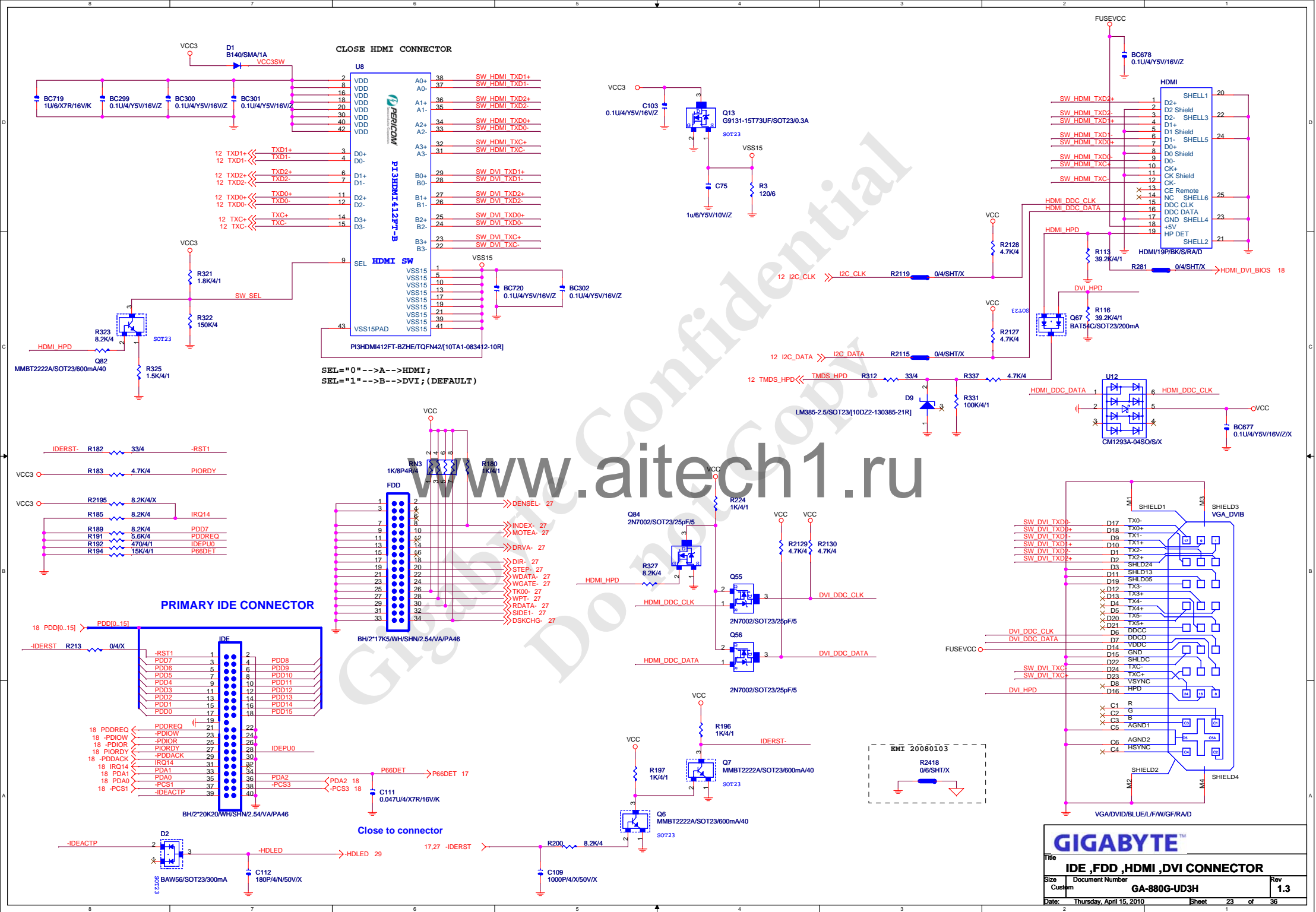
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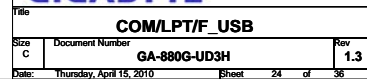
Sheet
20

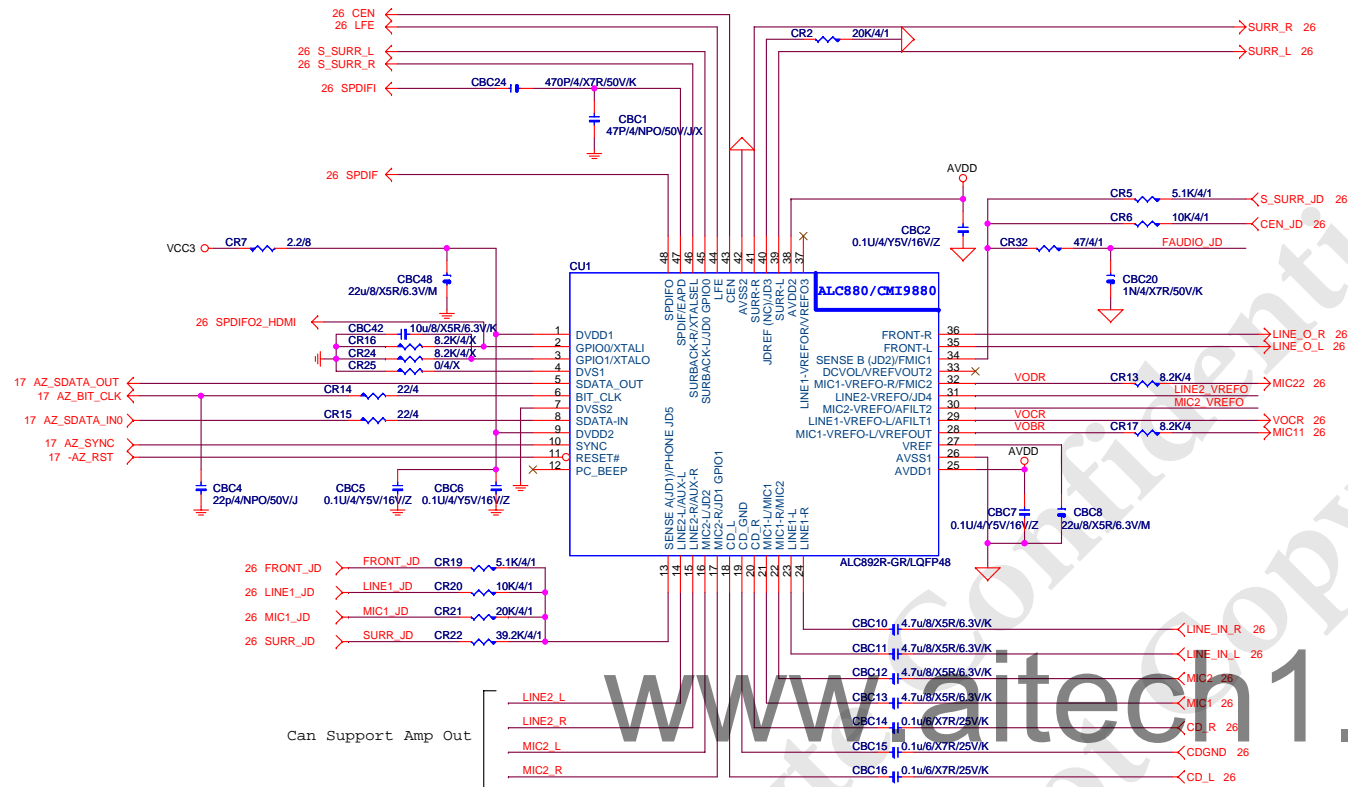
of
36

Rev
1.3

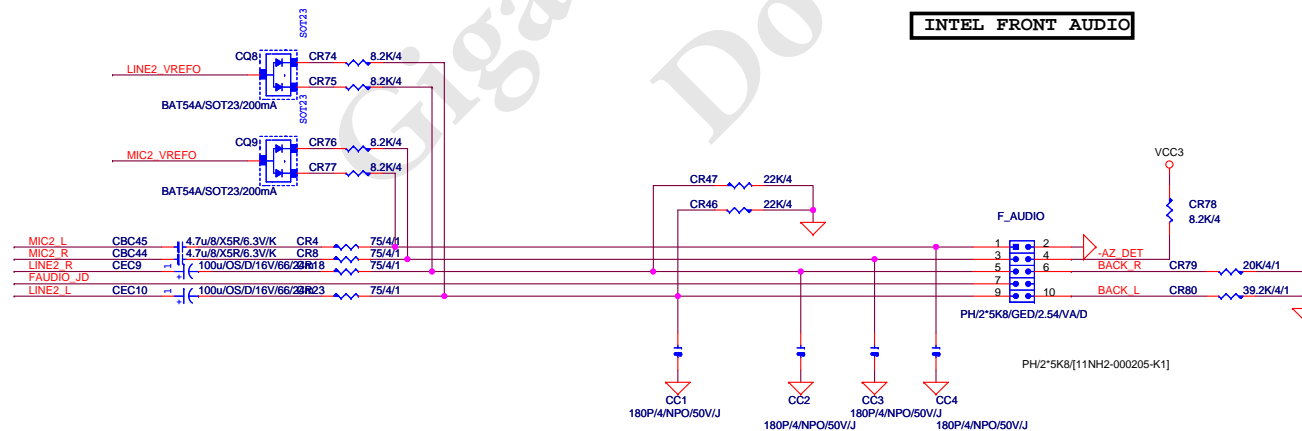








INTEL FRONT AUDIO

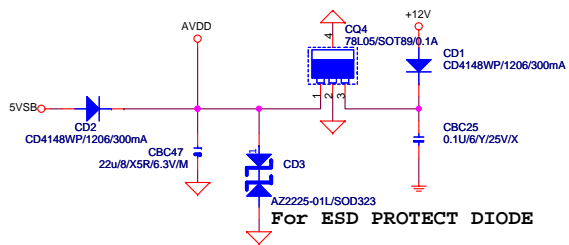
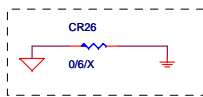


AZALIA CODEC ALC892R/ALC889A/ Colay

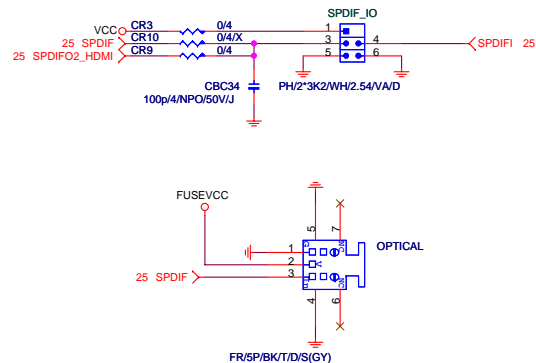
	ALC892R	ALC889A
CR16	X	O
CR24	X	O
CR25	X	O
CBC42	10uF/X5R	X
CR2	20K/1%	20K/0.1%
CR9	O	X
CR10	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR28/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	75 ohm

GIGABYTE

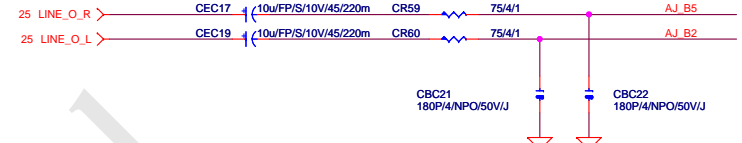
Title ALC892R CODEC		
Size Custom	Document Number GA-880G-UD3H	Rev 1.3
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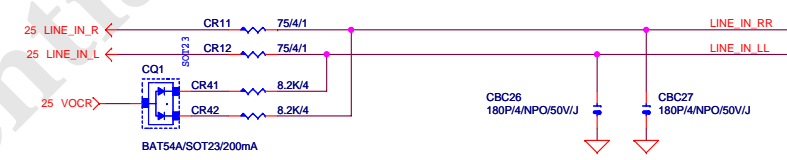
SPDIF



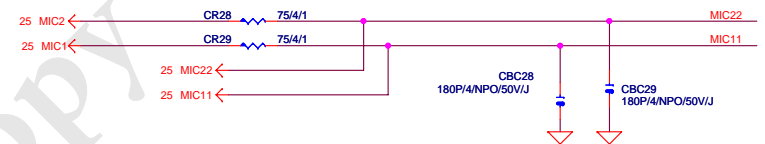
LINE OUT FRONT OUT



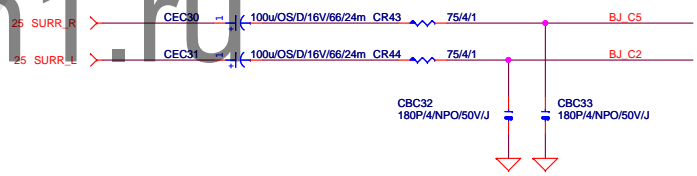
LINE-IN



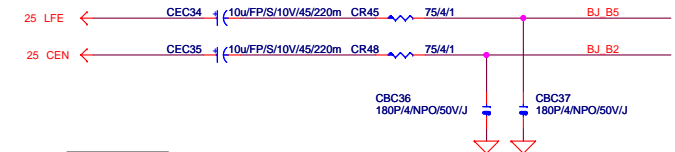
MIC



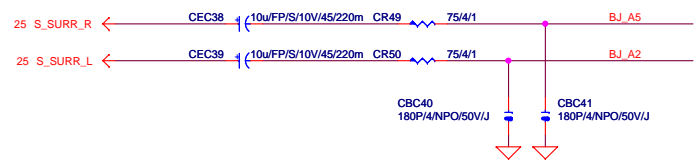
SURROUND



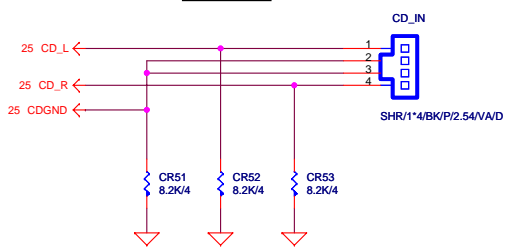
CEN/LFE



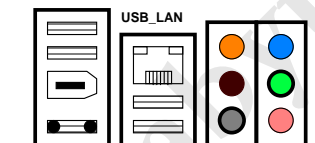
SURR BACK



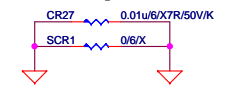
CD IN



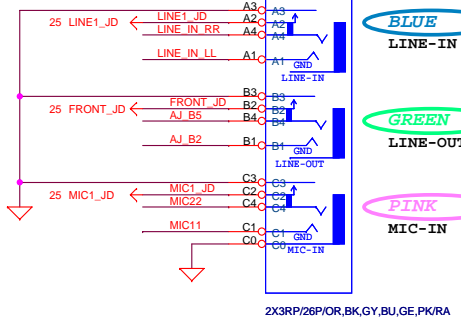
USB_1394_ESATA



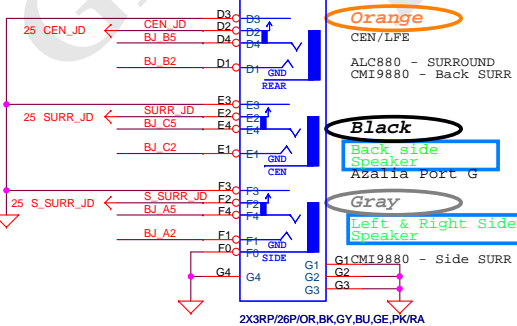
For Audio precision test



AUDIOB



AUDIOA



Orange

ALC880 - SURROUND
CMI9880 - Back SURR

Black

Back side
Speaker
Azalia Port G

Gray

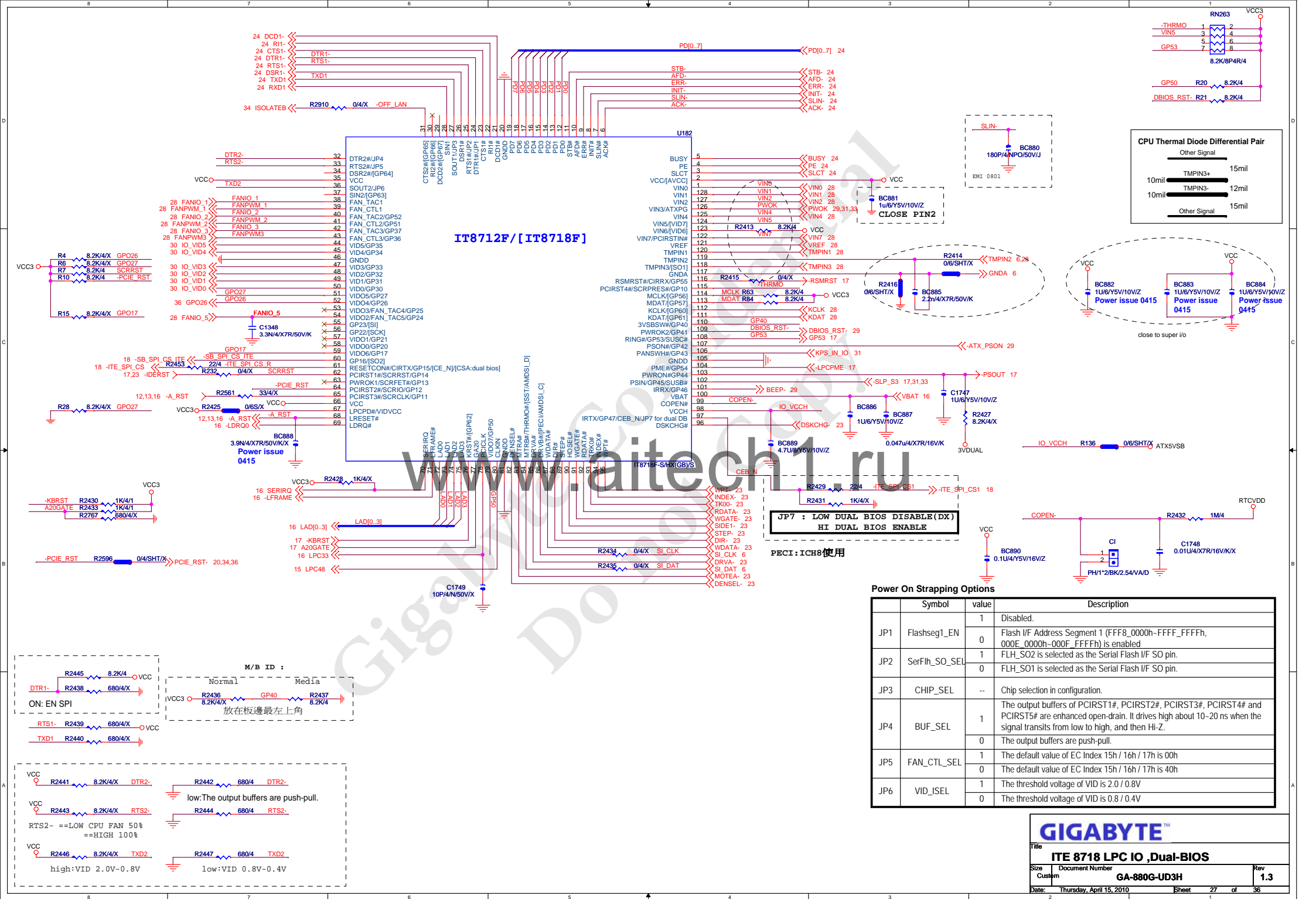
Left & Right Side
Speaker

G1CMI9880 - Side SURR

GIGABYTE™

AUDIO JACK

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27 VREF <<

27 TMPIN1 <<

27 TMPIN3 <<

6.27 TMPIN2 >>

C113
1u6/Y5V/10V/Z

C114
0.1u6/X7R/25V/K

R206
8.2K/4/X

RS1
10K/1/4/S

R203
10K/4/1

R205
10K/4/1

R2253
30K/4/X
FOR 8716 N/A

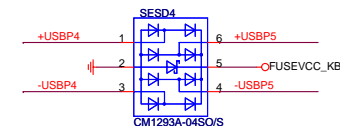
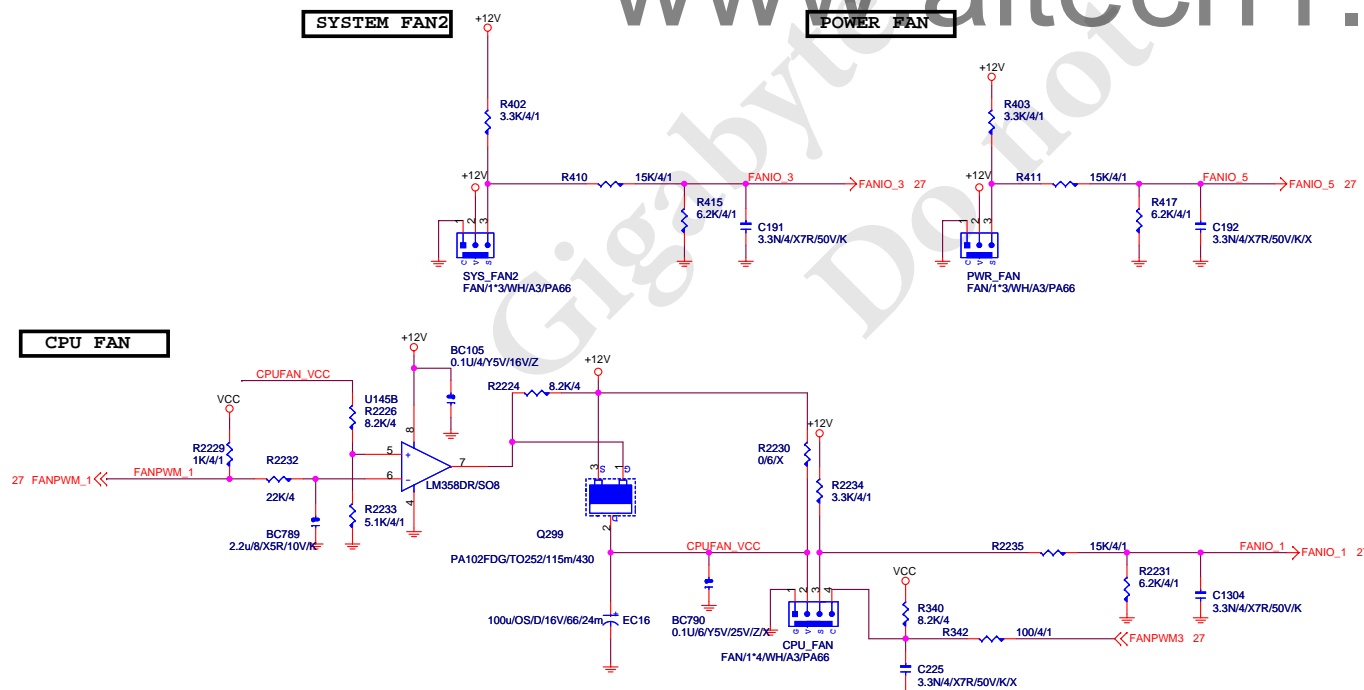
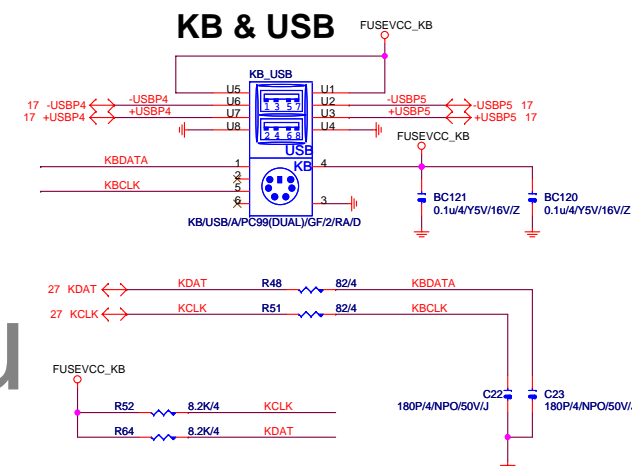
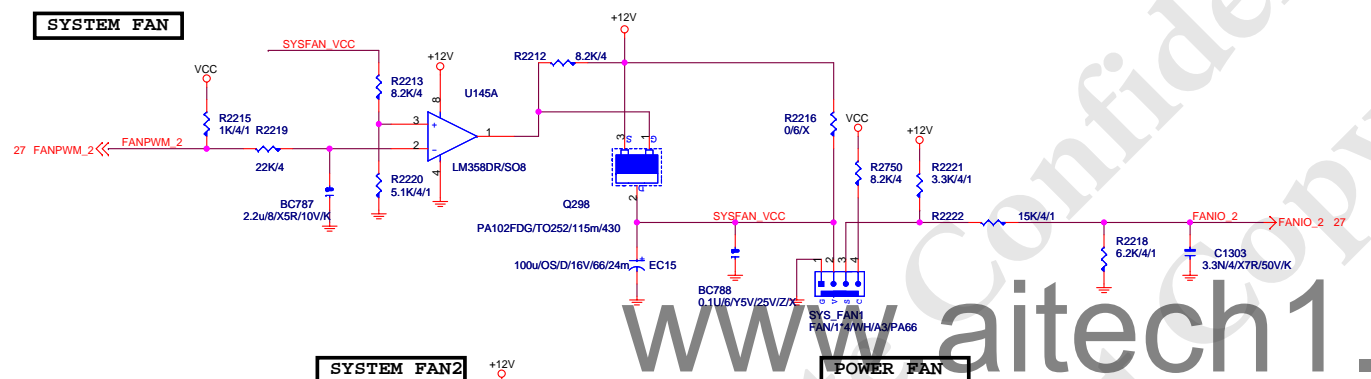
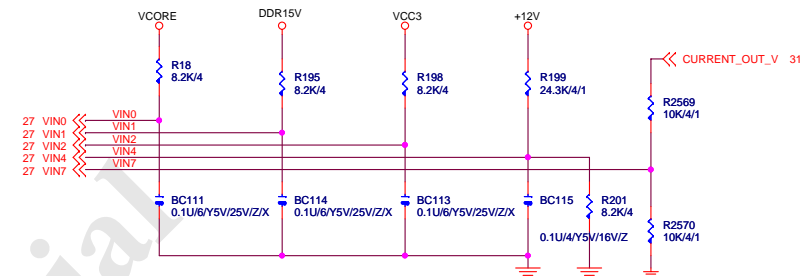
C1080
0.1u4/Y5V/16V/Z

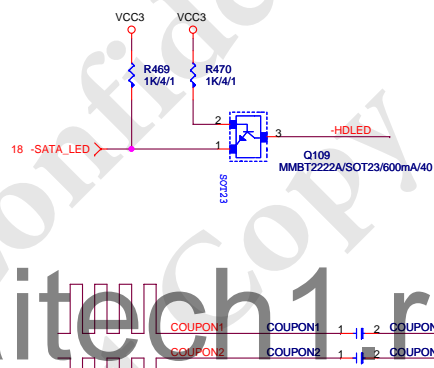
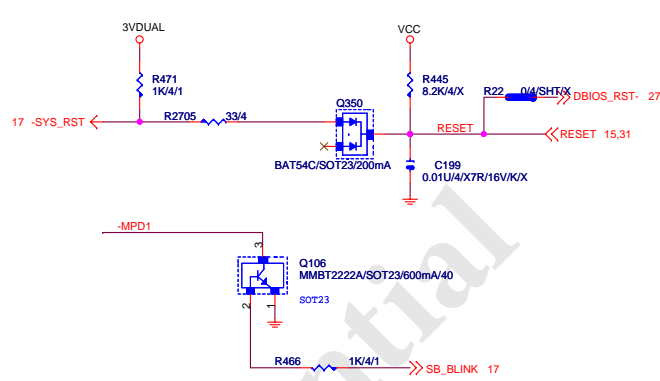
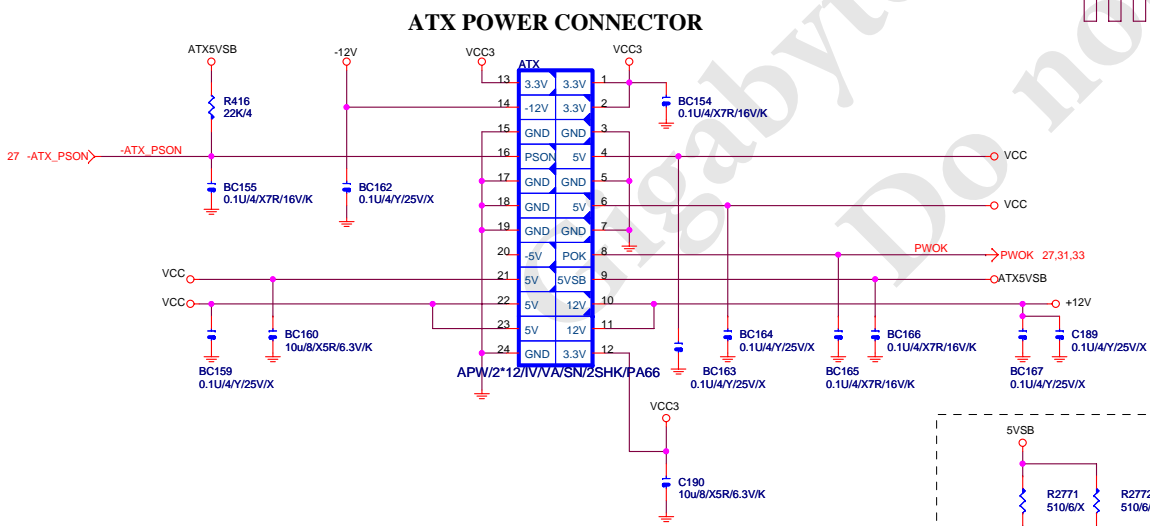
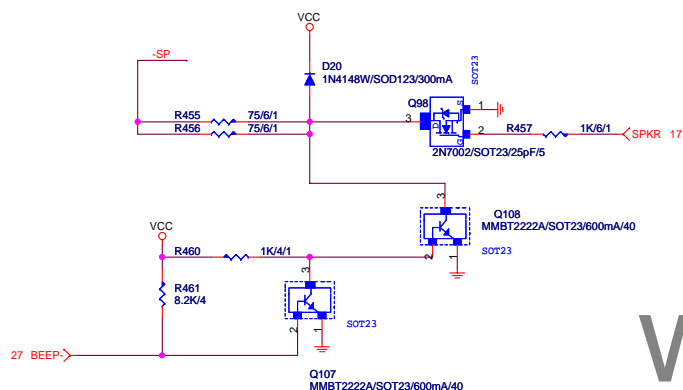
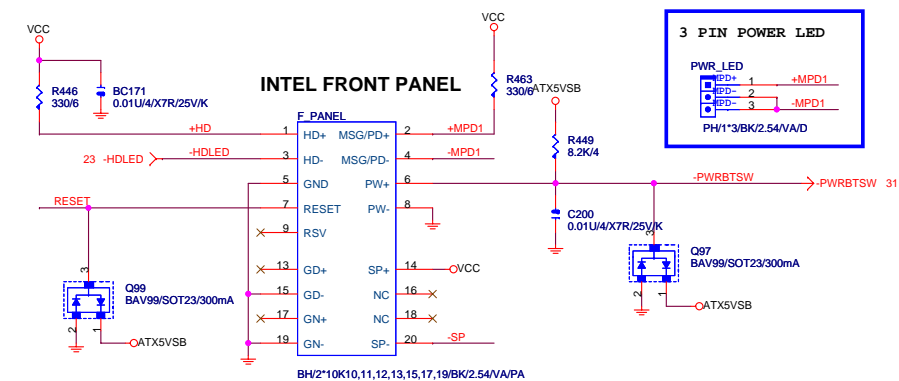
C1306
3.3N/4/X7R/50V/K

SYSTEM Thermister

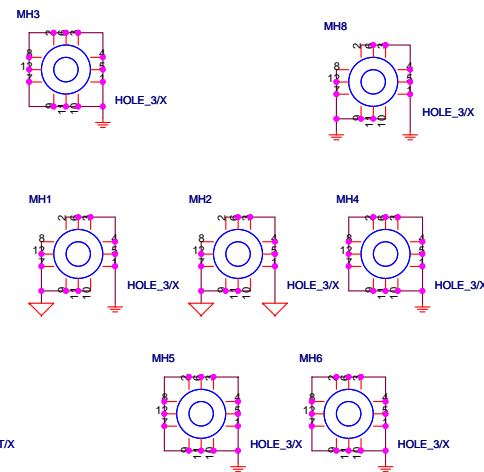
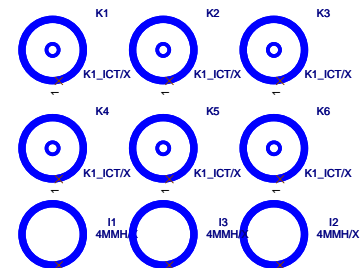
CPU Thermister

Ground symbol





For Seasonic 900W
Power supply
cant Boot issue



GIGABYTE™			
Title			
ATX, FRONT PANEL			
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The schematic diagram illustrates the test circuit for the BAW56 MOSFET. It features a 5VSB supply connected to a network of resistors (R2855, R2856, R2857, R2858) and a capacitor (C216). The circuit includes three MOSFETs: Q358 (MMBT2907A/SOT23/600mA/450), Q361 (MMBT2222A/SOT23/600mA/40), and Q14 (BAW56/SOT23/300mA). The output is labeled 5VDUAL. A P_GATE signal is connected to the gate of Q14.

5VDUAL

3VDUAL

C234
0.1uF/4Y5V16V/Z

C236
0.1uF/4Y5V16V/Z

EC40
560uF/FP/D6.3V/687mF

036
L1085/D7/0232/5A

R1735
100/4/1

R1737
150/4/1

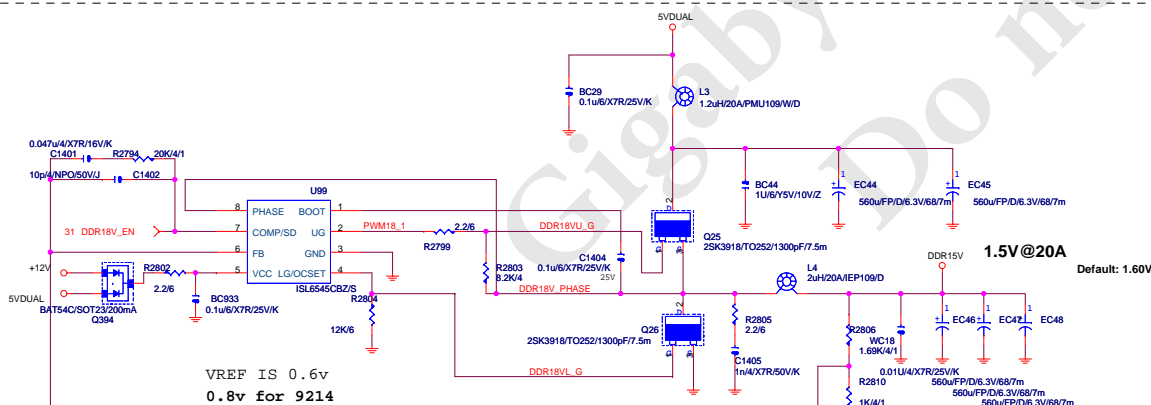
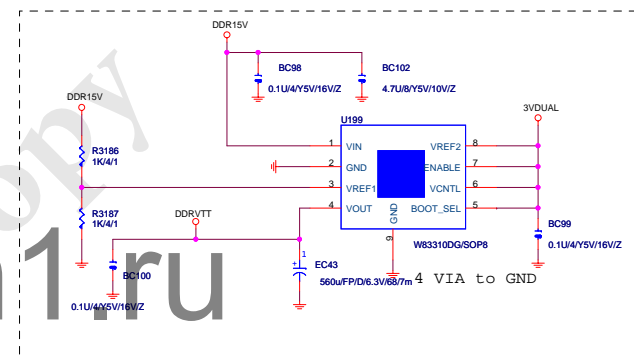
1

2

3

1.25V*(1+169/100)=3.36V

9.5V / 25A protect
 $9.5 \times (1.21K / (13.3K + 1.21K)) = 0.792V$



DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
L	X	X	X	1.65V
X	L	X	X	1.70V
L	L	X	X	1.75V
X	X	L	X	1.80V
L	X	L	X	1.85V
X	L	L	X	1.90V
L	L	L	X	1.95V

Default: 1.60V

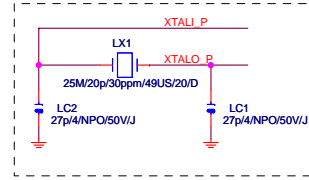
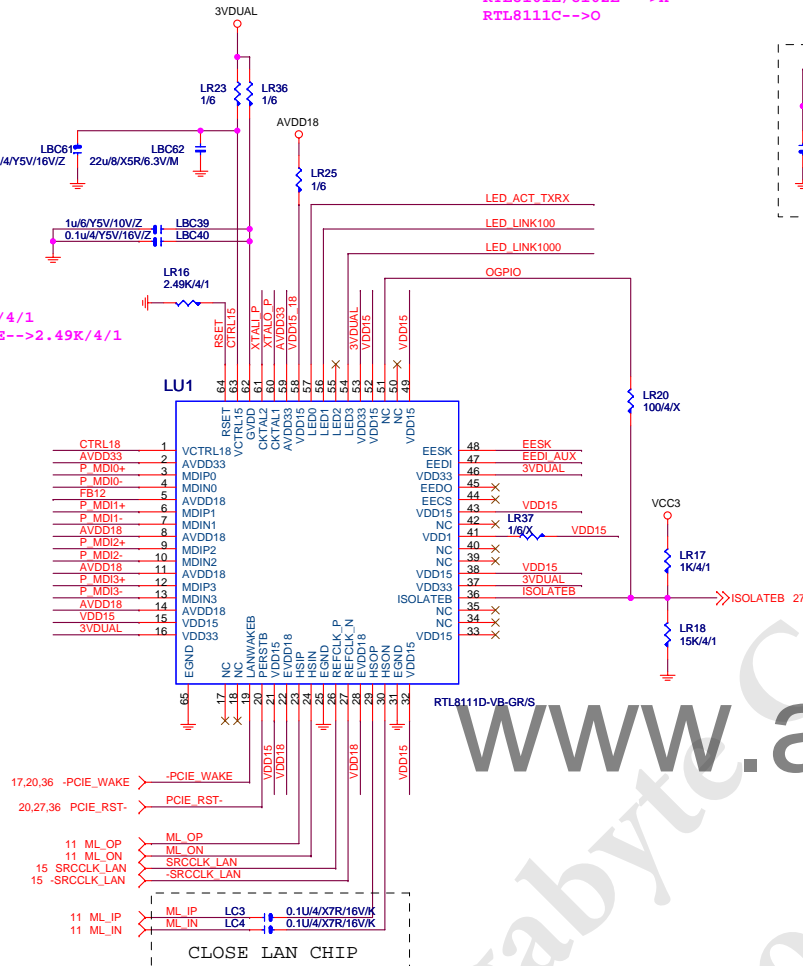
DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
X	X	X	L	2.00V
L	X	X	L	2.05V
X	L	X	L	2.10V
L	L	X	L	2.15V
X	X	L	L	2.20V
L	X	L	L	2.25V
X	L	L	L	2.30V
L	L	L	L	2.35V

PCIE-1G LAN

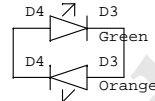
RTL8111C

LR36:
RTL8101E/8102E -->X
RTL8111C-->O

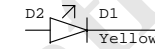
LR16:
RTL8101E-->2K/4/1
RTL8111C/8102E-->2.49K/4/1



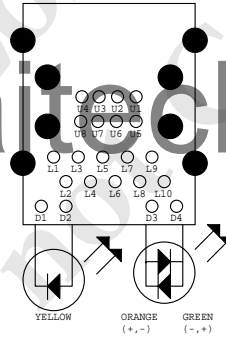
Dual Color LED



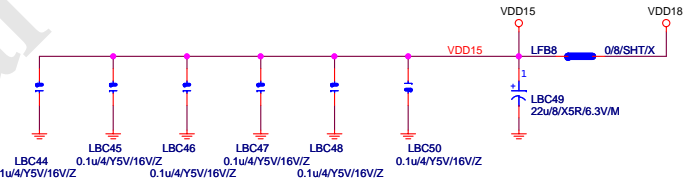
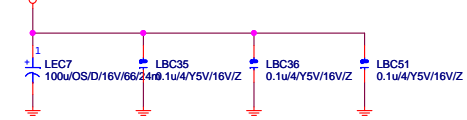
Single Color LED



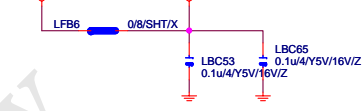
P35-152-19W9



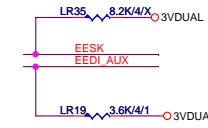
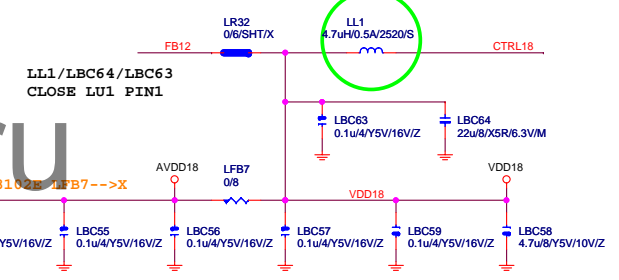
3VDUAL



3VDUAL



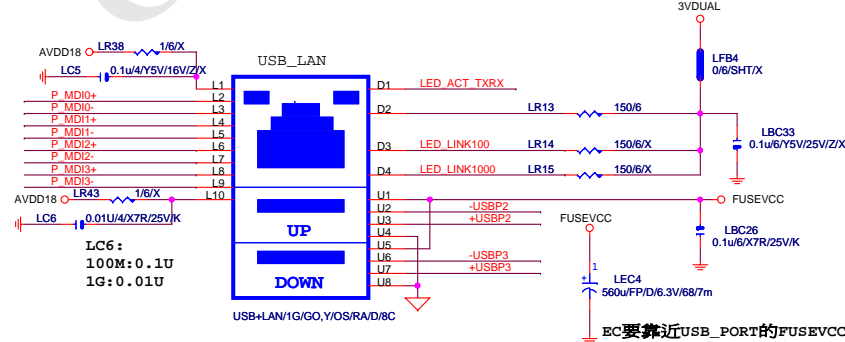
CHOKE4U7-500MA



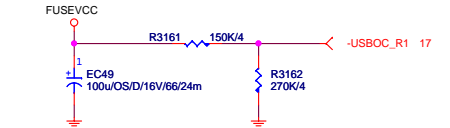
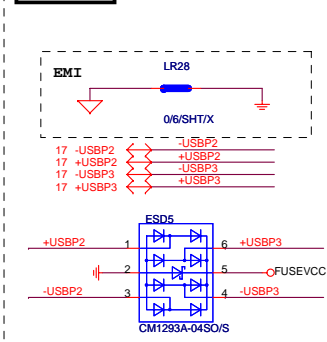
USB_LAN CONNECTOR

RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8102E:LC5/LC6-->O
RTL8111C:LC6-->O

RTL8102E -->X



USB_LAN



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REALTK RTL8111D			
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